WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate;

a dielectric layer overlying the semiconductor substrate;

a continuous conductor disposed on the dielectric layer; and

wherein the semiconductor substrate defines an aperture therein in at least a portion of a region underlying the continuous conductor.

2. The semiconductor device of claim 1 further comprising substantially vertical first and second conductive vias in the dielectric layer, wherein the continuous conductor comprises first and second terminal ends, and wherein the semiconductor substrate comprises active regions, and wherein the first and the second conductive vias electrically connect an active region to the first and the second terminal ends, respectively.

3. The semiconductor device of claim 1 wherein a material of the continuous conductor comprises aluminum.

4. The semiconductor device of claim 1 wherein the continuous conductor comprises an inductor.

5. The semiconductor device of claim 1 wherein a size and a geometrical pattern of the continuous conductor provides a desired inductance value.

6. The semiconductor device of claim 1 wherein the continuous conductor comprises a spiral shape.

7. The semiconductor device of claim 1 further comprising a dielectric material disposed within the aperture.

8. The semiconductor device of claim 1 further comprising a material disposed within the aperture selected from between a non-conductive and a non-semiconductive material.

9. The semiconductor device of claim 1 wherein the semiconductor substrate further comprises an upper and a lower surface, and wherein the aperture extends from the upper surface to the lower surface in the region underlying the continuous conductor.

10. An semiconductor device comprising:

a semiconductor substrate;

a plurality of active regions formed in the semiconductor substrate;

a dielectric layer overlying the semiconductor substrate;

one or more conductive interconnect layers overlying the dielectric layer;

a continuous conductor formed in one of the conductive interconnect layers; and

wherein the semiconductor substrate defines an aperture therein in a region underlying the continuous conductor.

11. The semiconductor device of claim 10 wherein at least one of the one or more conductive interconnect layers underlying the continuous conductor defines an aperture therein in a region underlying the continuous conductor, and wherein a material selected from between a non-conductive material and a non-semiconductive material is disposed within the aperture.

12. The semiconductor device of claim 10 further comprising a dielectric layer disposed between successive layers of the one or more conductive interconnect layers.

13. The semiconductor device of claim 10 further comprising conductive vias, wherein the continuous conductor comprises first and second terminal ends, and wherein the conductive vias electrically connect each of the first and the second terminal ends to one of the plurality of active regions.

14. The semiconductor device of claim 10 further comprising conductive vias, wherein the continuous conductor comprises first and second terminal ends, and wherein the conductive vias electrically connect each of the first and the second terminal ends to one of the one or more conductive interconnect layers.

15. The semiconductor device of claim 10 further comprising first and second conductive vias, wherein the continuous conductor comprises first and second terminal ends, and wherein the first conductive via electrically connects the first terminal end to one of the plurality of active regions, and wherein the second conductive via electrically connects the second terminal end to one of the conductive interconnect layers.

16. The semiconductor device of claim 10 further comprising a material disposed within the aperture selected from between a non-conductive and a non-semiconductive material.

17. A semiconductor device comprising:

a semiconductor substrate having active regions formed therein;

a dielectric layer overlying the semiconductor substrate;

conductive vias formed in the dielectric layer extending between an upper surface of the dielectric layer and an active region;

conductive lines comprising an inductor formed overlying the upper surface and further comprising first and second terminal ends, wherein each of the first and the second terminal ends is in electrical communication with a conductive via; and

wherein the semiconductor substrate comprises an aperture underlying at least a portion of the conductive lines.

18. The semiconductor device of claim 17 wherein a material disposed within the aperture is selected from between a dielectric material and a bonding material.

19. The semiconductor device of claim 17 wherein a material disposed within the aperture comprises one of a non-conductive material and a non-semiconductive material.

20. The semiconductor device of claim 17 wherein the semiconductor substrate further comprises an upper and a lower surface, and wherein the aperture extends from the upper to the lower surface underlying at least a portion of the conductive lines.

21. A method for forming an inductor, comprising;

forming a semiconductor substrate;

forming a dielectric layer overlying the substrate, wherein the dielectric layer comprises an upper surface;

forming conductive lines on the upper surface, wherein the conductive lines exhibit an inductive effect; and

removing a region of the semiconductor substrate underlying at least a portion of the conductive lines.

22. The method of claim 21 further comprising forming active regions in the semiconductor substrate.

23. The method of claim 21 wherein the conductive lines comprise first and second terminal ends, further comprising forming conductive interconnects

through the dielectric layer for connecting the first and the second terminals to active regions.

24. The method of claim 21 wherein the step of removing a region of the semiconductor substrate comprises etching the semiconductor substrate.

25. The method of claim 21 wherein the step of removing a region of the semiconductor substrate comprises micro-machining the semiconductor substrate.

26. A method for forming an inductor, comprising;

forming a semiconductor substrate;

forming one or more dielectric layers overlying the substrate, wherein an upper layer of the one or more dielectric layers comprises an upper surface;

forming conductive lines on the upper surface, wherein the conductive lines exhibit an inductive effect; and

defining an aperture by removing a region of one or more of the dielectric layers underlying at least a portion of the conductive lines.

27. The method of claim 26 further comprising depositing a dielectric material in the aperture.